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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/702,615	11/07/2003	In Duk Song	8733.930.00-US	8495

30827 7590 02/17/2006

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EXAMINER	
KIM, RICHARD H	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 02/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/702,615	SONG ET AL.	
	Examiner	Art Unit	
	Richard H. Kim	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *5-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12 and 104* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 9, 10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ono et al. (US 6,726,802 B2).

As to claim 1, Ono et al. discloses a plurality of gate lines aligned on the substrate, a plurality of data lines crossing the gate lines to form a plurality of pixel regions (Fig. 17, ref. GL, DL); a thin film transistor located at the intersection of a gate line and a data line (TFT); a pixel electrode located in each pixel region (PX), wherein the array substrate includes a storage capacitor comprising a lower storage electrode across the data line and in parallel with the gate line on the same layer as the gate line (Fig. 17, ref. CT(g1); col. 21, lines 14-15), wherein the lower storage electrode divides the pixel region into two sub-regions (Fig. 17, ref. CL), and a semiconductor layer interposed between the lower storage electrode and the pixel electrode (Fig. 17, ref. AS).

As to claim 2, Ono et al. discloses that the pixel electrode is connected to the semiconductor layer by a through hole formed on an upper region of the semiconductor layer (Fig.16, AS, PX).

Referring to claim 4, Ono et al. discloses that only the semiconductor layer and a gate insulating layer are interposed between the lower storage electrode and the pixel electrode (GI, AS).

Referring to claim 9, Ono et al. discloses a gate line (GL), a gate electrode (GL), and a lower storage capacitor (Cstg); an insulating layer (GI) on the substrate having the gate line, gate electrode, and lower storage electrode, a semiconductor layer (AS) on the lower storage electrode, a data line (DL) on the substrate having the insulating layer; a protection layer (PSV2) on the substrate having the data line, the protection layer having a contact hole (CN) above a part of the semiconductor layer; and a pixel electrode on the protection layer (PX), wherein the pixel electrode contacts the top of the semiconductor layer, wherein the gate line and data line cross to form a pixel region; and wherein the storage electrode is parallel to the gate line and divides the pixel region into two sub-regions (Fig. 17, ref. CL).

As to claim 10, Ono et al. discloses that the pixel electrode is connected to the semiconductor layer by a through hole formed on an upper region of the semiconductor layer (Fig. 21, ref. AS, PX).

Referring to claim 12, Ono et al. disclose that only the semiconductor layer and a gate-insulating layer are interposed between the lower storage electrode and the pixel electrode (GI, AS).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al.

Ono et al. discloses the device previously recited, and further discloses that the semiconductor layer is inside the pixel region (Fig. 17, ref. AS). However, the reference fails to disclose that the semiconductor layer is at least as wide as the lower storage electrode.

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the semiconductor region to be at least as wide as the lower storage electrode since Ono et al. discloses that the semiconductor layer increases the charge holding capacitance value per area (col. 24, lines 24-25). Therefore, increasing the width, in order to increase the charge holding capacitance is a result effective variable and requires only routine skill in the art.

Response to Arguments

5. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard H. Kim whose telephone number is (571)272-2294. The examiner can normally be reached on 9:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard H Kim
Examiner
Art Unit 2871

RHK

ANDREW SCHECHTER
PRIMARY EXAMINER